A LCD Controller which Supports A No-Scaling Image Without a Frame Buffer

Background of the Invention

Field of the Invention

This invention relates to a method and apparatus for providing liquid crystal display LCD control. More particularly this invention relates to a method and apparatus for displaying unscaled images on LCD panels without a frame buffer. The method and apparatus uses the same buffers available to the digital signal processor DSP for displaying the image.

Description of Related Art

Today, conventional LCD controllers utilize a scaling up mapping. Figure 1 shows a mapping of a 640 by 480 pixel image 110 being displayed on a 1024 by 768 pixel LCD display 120. The figure illustrates a scaling up of the image to fit the LCD display, which has a larger pixel format(1024 by 768) than the image (640 by 480). The mappings 130 & 140 of the starting and finishing points of the image are shown in Fig. 1. The conventional circuit to perform the above scaling up operation requires a higher clock frequency to produce a display on the LCD panel. This higher frequency is required for the scaling up digital signal processor, DSP to keep the same frame rate as the smaller image. In addition, this convention implementation needs several line buffers for temporary data storage.

Figure 2 shows the conventional implementation of the No-scaling LCD display. In this case, a frame buffer is required to capture the whole frame of image data so that the 640 by 768 image 210 can be displayed anywhere on the LCD panel's 1024 by 768 grid 220. The mappings 230 & 240 of the starting and finishing points of the image are shown in Fig. 2. A example to illustrate the conventional method's requirement for a frame buffer. If the source image is 640 x 480 and the LCD panel is 1024 x 768, the source frame time provided without a frame buffer would be defined by 480 Hsync pulses and the LCD image frame time is given by 768 Hsync pulses. The reason why the frame buffer must be used is because the frame time for the source image has to equal that of the entire larger LCD frame. However, the available frame time for the non-scaled display image is significantly less than that of the source image as illustrated above by the difference in the number of Hsync pulses.

U. S. Patent 5,537,128 (Keene, et al.) "Shared Memory for Split-Panel, LCD Display Systems" describes a memory sharing method for a split panel LCD. The method enables efficient memory sharing and video processor usage between an LCD driver and a CRT driver in a common system.

U. S. Patent 5,712,681 (Suh) "Apparatus for Inputting and Outputting an Optical Image with Means for Compressing or Expanding the Electrical Video Signals of the Optical Image" shows an apparatus capable of inputting and

outputting an optical image. A means of compressing or expanding the electrical video data is provided. The circuit displays the captured image on an LCD panel.

U. S. Patent 6,049,322 (Yoshikawa et al) "Memory Controller for Liquid Crystal Display Panel " provides a memory controller for an LCD panel. The apparatus allows the source driver for the LCD to operate at a lower frequency than the line buffer.

Brief Summary of the Invention

It is the objective of this invention to provide a method and an apparatus to display a source image on a LCD panel without scaling.

It is further an object of this invention to provide this LCD display using lower clock frequencies than would normally be required using the scale up display methods of the present art.

In addition, it is further the object of this invention to display on a LCD panel without the use of a frame buffer.

The objects of this invention are achieved by a method to display a source image on a LCD panel without scaling. The method begins by transferring the even image line to line buffers. This is followed by the transferring the output of these line buffers to the input of the LCD panel drivers of the upper half portion within the LCD panel. Next, the method requires the skipping of the LCD Vsync at the end of a display within the even image lines. Then, there is the transferring the odd image lines to line buffers and the transferring the output of these line buffers to the input of the LCD panel drivers of the lower half portion within the LCD panel. Finally, the method requires the blanking of the data of the odd image of this lower portion of the LCD screen.

The objects of this invention are also achieved by an apparatus to display a source image on a LCD panel without scaling. This apparatus contains a means for transferring the even image line to line buffers and a means for transferring the output of these line buffers to the input of the LCD panel drivers of the upper

half portion within the LCD panel. In addition, the apparatus contains a means for skipping the LCD Vsync-pl at the end of a display within the even image lines. There is also a means for transferring the odd image lines to line buffers and for transferring the output of these line buffers to the input of the LCD panel drivers of the lower half portion within the LCD panel. Finally, the apparatus contains a means for blanking the data of said odd image of said lower portion of the LCD screen.

Brief Description of the Drawings

FIG. 1 shows a prior art scaling up mapping.

FIG. 2 shows a prior art no-scaling up mapping.

FIG. 3 shows the no-scaling up mapping algorithm of this invention Step 1.

FIG. 4 shows the no-scaling up mapping algorithm of this invention Step 2.

FIG. 5 shows the no-scaling up mapping algorithm of this invention (Step 3).

FIG. 6 shows the Vsync, Hsync Timing diagram.

FIG. 7 shows how movement of Vsync varies the position of the image display on the LCD.

Detailed Description Of The Invention

Fig. 3 shows the first steps of the method of this invention. The even image lines 310 are mapped to the LCD panel. This figure shows the mapping of a no-scaling algorithm. The same number of line buffers are used for this mapping as is used in the traditional scaling algorithm. The digital signal processor, DSP, needs to implement and produce the non-scaling image on the LCD panel. The output of the DSP goes to the line drivers, which drive the cells of the LCD panel. The starting and finishing points of the even image lines are mapped 330, 340 to the LCD panel as shown in figure 3. The odd image lines are mapped 350 directly below the upper even lines.

Figure 4 shows the next step of the method. The source 410 image and the LCD panel 440 are shown. The even image lines 420 are displayed and visible on the LCD panel. The odd image lines are blanked or not displayed 430. This method requires that one frame of data, the odd frames, is skipped every other frame. Since the odd source lines are directly adjacent to the even source lines, eliminating the odd scan lines results in minimal loss of information. While the embodiment shows a non-scaled image that occupies about half of the display panel, in general, the invention will work with various fractional sizes of the display. For example, the non-scaled image might occupy 2/3 of the display. Any source resolution smaller than the display resolution will work.

Figure 5 shows the final steps of the method. The source 510 image and the LCD panel 530 are shown.The mappings 540, 550 of the starting 560 and

finishing 570 points of the image to the LCD panel are shown. The non-scaled display of the image on the LCD panel is shown 520. Comparing figures 4 and 5, the shift of the image display on the LCD panel is noticed. In figure 4, the displayable image 420 is shifted to the top of the LCD panel 440. In figure 5, the displayable image 520 is centered on the LCD panel 530. This shifting and centering of the image on the LCD panel is accomplished by shifting the vertical synchronization Vsync signal of the LCD panel. In this case, the Vsync signal is shifted to the left on the time domain timing diagrams.

Figure 6 shows the time domain timing diagram. This diagram illustrated the source image buffer data_source 610, Hsync_source 620, and Vsync_source 630 signals. It also shows the LCD panel data_panel 640, Hsync_panel 650, and Vsync_panel 660 signals. The even image data 670 and the odd image data 680 are shown. However, on the LCD panel, the even data 690 is displayed while the odd data 691 is blanked out or not displayed. This is accomplished by skipping every other Vsync signal 615, 625 on the LCD panel. When a Vsync signal is skipped, the next odd frame of data is not begun at the normal starting point at the upper left of the displayable area on the LCD. Consequently, the present set of even image lines remains visable on the LCD panel.

In addition, moving the position of the even frame Vsync signals 635, 615, 655 controls the position of the image display on the LCD panel. The movement of the Vsync 635 to the left moves the image display downward. While movement of the Vsync 635 to the right moves the image display upward.

Figure 7 further illustrates how the movement of the Vsync signal controls the position of the image display up or down on the LCD panel. Fig. 7 shows the blanked out areas 701, 703 of the display data as well as the even frames of displayable data 702, 704. There are three cases illustrated in figure 7. Case 1 shows the Vsync pulse lined up with the transition from blank data to Even frame displayable data 710. The corresponding LCD image display showing the displayable image starting at the top of the LCD 720. Case 2 shows the Vsync pulse occuring in the middle of the blank data 730. The corresponding LCD image display showing the displayable image centered in the middle of the LCD 740. Case 3 shows the Vsync pulse lined up with the transition from even displayable data to bland data 750. The corresponding LCD image display showing the displayable image skewed toward the bottom of the LCD 760.

Figure 6 also illustrates that the frequency of the Vsync of the LCD panel is one half of the frequency of the Vsync of the source. Also, the frequencey of the horizontal synchronization signal Hsync of the LCD panel 650 equals the Hsync of the source 620. Therefore, the Vsync frequency requirements are equal to or less than those of the source.

This invention has the advantage of lower cost since extra frame buffers are not required. In addition, the circuits and apparatus required to implement the method of this invention are relatively simple. They involve halving the frequency of the Vsync signal. In addition, the circuitry is required to move the

position of the Vsync signal to establish the position of the displayed image on the LCD panel.

While this invention has been particularly shown and described with Reference to the preferred embodiments thereof, it will be understood by those Skilled in the art that various changes in form and details may be made without Departing from the spirit and scope of this invention.

What is claimed is: